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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/409,940	09/30/1999	BRYAN KEITH BULLIS	RAL9-99-0056	6159

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EXAMINER	
FERRIS III, FRED O	
ART UNIT	PAPER NUMBER
2123	

DATE MAILED: 02/20/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/409,940	Applicant(s) BULLIS ET AL.	
	Examiner Fred Ferris	Art Unit 2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on *10 December 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on *10 December 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. *Claims 1-23 have been presented for examination based on Applicant's amendment filed on 10 December 2002. Claims 1-23 remain rejected by the examiner.*

Response to Arguments

2. *Regarding Declaration under 37 CFR 1.132 and 112(1) rejection: The Declaration under 37 CFR 1.132 filed 10 December 2002 is insufficient to overcome the rejection of claims 1-23 based upon the opinion of the inventor, as set forth in the last Office action because: The Declaration has introduced new matter which should have been incorporated into the specification in order to clearly define the claimed invention in exact terms and provide enablement for the claims. Specifically, the Declaration discloses on pages 3-7, and in Exhibit A and B, matter relating to the operation of the "snooper", "generator", "interface, and "checker" which would be required by one of ordinary skill in the art to make and or use the invention. Accordingly, the examiner maintains the 112(1) rejection since the specification does not adequately disclose the invention and does not provide enablement for the claims.*

Regarding objection to the drawing: Applicant's drawings submitted on 10 December 2002 have been approved by the examiner.

Regarding applicant's response to 102(e) rejections: Applicant's arguments with respect to claims 1-23 have been considered but are moot in view of the new ground(s) of rejection. (see 103(a) rejection)

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

*3. Claims 1-23 rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which **is not described in the specification** in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.*

Specifically, regarding independent claim 1: Claim 1 is drawn to a system for providing simulation of an integrated circuit consisting of:

*A **snooper** coupled with **the interface** for obtaining an **output** by the island.*

*A **checker** coupled with **the interface** for checking whether output is **desired output**.*

*A **generator** coupled with **the island** for providing an **input** to the island.*

*The specification of the claimed invention does not adequately disclose the operation of the claimed "**snooper**" or "**the interface**" in a way that would allow one skilled to art to make and/or use it. The specification makes reference to the snooper being "coupled with an interface" and being for "obtaining an output provided by the island during simulation and forwarding the information to the checker" but does not disclose an algorithm or technique for the implementation of either the "snooper" or "the interface".*

When "snoopers" are used in electronic systems, they are generally realized in either hardware or software. For example, software "snoopers" are can be employed by

the resource manager of a communication network for purposes such as the extraction and verification of information relating to ID packets. Hardware "snoopers" are generally comprised of control logic, address sequencer, data sequencer, timing signals, and latch-and-hold circuits, and perform a similar function but are typically used for monitoring and verifying hardware status.

If the claimed "snooper" is realized in software, then an algorithm and flow chart of the "snooping" process should be disclosed. If the "snooper" is realized in hardware then a block diagram and hardware description should be provided.

The specifics of the claimed "interface" is also not disclosed in the specification. While numerous industry standard electronic interfaces such as RS-232, IEEE-488, VME, etc. do exist, the applicants have not identified a standard interface nor have they disclosed their own design. The specifics of the claimed "interface" appear to be critical matter relating to the operation of the claimed invention and needs to be disclosed in detail.

The claimed "checker" is further not disclosed by the specification in a way that would allow one skilled in the art to make and/or use it. The specification references the checker being "coupled with the interface" and that it is for "checking the outputs to determine whether the outputs are desired outputs" but does not disclose how the checker performs the claimed "checking" of the output and does not disclose what constitutes a "desired output".

The claimed "generator" is also not disclosed by the specification in a way that would allow one skilled in the art to make and/or use it. Reference is made to the

"generator" and being "coupled with an interface for providing inputs or outputs to the island" and usually "directed by a test case, but no description of the interface coupling or the related inputs and outputs is provided. Further, no description or explanation of how the generator is "directed by a test case" is given and there is no description of how the generator actually functions.

Dependent claims 2-9 inherit these defects.

Regarding independent claim 10: Claim 10 is drawn to a method for providing simulation of an integrated circuit consisting of the steps of:

***Snooping** the **interface** to obtain an output by the island.*

***Checking** the output to determine whether the **output is desired**.*

***Providing** an input to the island during simulation.*

Directing** the providing of the input using a **test case.

*As previously described the specification of the claimed "**snooper**", "**interface**", "**checker**", "**generator**", "**test case direction**", or the related **steps** involved in each process (i.e. "snooping", "checking" etc.) in a way that would allow one skilled to art to make and/or use it. Accordingly, independent claim 10 is rejected as described above.*

Dependent claims 11-16 inherit these defects.

Regarding independent claim 17 and dependent claims 18-23: Claims 17-23 are directed toward the computer readable medium and program instructions for the features outlined in claims 1-16 and are rejected using the reasoning as disclosed above.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

4. ***Claims 1-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 6,182,258 issued to Hollander in view of U.S. Patent 6,006,024 issued to Guruswamy et al.***

While the specification regarding the claimed invention is delinquent in the areas cited in the 35 U.S.C. 112(1) rejections section of this office action the examiner has made prior art rejections based on the limited scope of information contained in the specification for supporting the claims.

Independent claim 1 is drawn to a system for providing ***simulation*** *of an* ***integrated circuit*** *consisting of:*
A ***snooper*** *coupled with* ***the interface*** *monitoring island* ***output****.*
A ***checker*** *coupled with* ***the interface*** *for checking whether output is* ***desired output****.*

*A **generator** coupled with **the island** for providing an **input** to the island.*
*A **test case** directing generator to determine output based on input, intelligence to provide input based on request, generator performs particular simulation.*

*Regarding independent claims 1, 10, and 17: Hollander teaches a system, method, and computer code for functionally verifying an integrated circuit design that monitors (i.e. **snoops**) the **simulation** of an **integrated circuit** design via a **checker** (with an **interface**) and including a **test generator** **using a** **test case** **which includes** **automation** (i.e. **intelligence** for directing test) for determining the defective behavior (for **desired output**) of the circuit in a semiconductor. (Abstract, Summary of Invention, CL3-L37, CL4-L66-CL5-L7, CL8-L30, CL10-L21, Figs. 1-5)*

In the abstract Hollander recites:
"The invention is platform and simulator-independent, and is adapted for integration with Verilog, VHDL, and C functions. A modular system environment ensures interaction with any simulator through a unified **system interface** that supports multiple external types. A **test generator** module automatically creates **verification tests** from a functional description. A test suite can include any **combination of statically and dynamically-generated tests.** Directed generation constrains generated tests to specific functionalities. Test parameters are varied at any point during generation and random stability is supported. A **checking module** can perform any combination of static and dynamic checks."

*Hollander does not explicitly teach verification (testing) a substrate incorporating cells via an **island**.*

*Guruswamy teaches a **cell layout generation** system environment that includes **islands** for an integrated circuit design. (Abstract, Detailed Description, CL9-L29, CL50-L30-65, Figs. 1-5, 60-67)*

It would have been obvious to one having ordinary skill in the art at the time the claimed invention was made to modify the teaching of Hollander relating to a system for

*functionally verifying an integrated circuit design that monitors (**snoops**) the **simulation** of an **integrated circuit** design via a **checker** and including a **test generator using a test case**, with the teachings of Guruswamy relating to a **cell layout generation** system environment that includes **islands** for an integrated circuit design to realize the claimed method for self-checking in an ASIC design. From a motivational standpoint, it further would have been obvious to apply the well known integrated circuit hardware verification techniques (i.e. "monitor (snooper)", "generator", "interface, and "checker") as taught by Hollander and simply include an **interface** to the **island** of an ASIC design to provide test case input and output data during simulation.*

*Regarding dependent claims 2-9, 11-16, 18-23: Hollander teaches a system where the **checker** incorporates and **interface** (**coupled**) to monitor (i.e. **snooper**) and **automatic test generator** for use in **integrated circuit** design where the generator and checker are obviously **reusable**. Hollander also teaches that the use a **test case** in monitoring the operation of an integrated circuit simulation. (Abstract, Summary of Invention, CL3-L37, CL4-L66-CL5-L7, CL8-L30, CL10-L21, Figs. 1-5)*

Conclusion

*4. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).*

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure, careful consideration should be given prior to applicant's response to this Office Action.

U.S. Patent 6,157,972 issued to Newman et al teaches snooper use in ASIC design.

U.S. Patent 5,958,011 issued to Arimilli et al teaches circuit simulation and snooper use.

U.S. Patent 6,292,931 issued to Dupenloup teaches ASIC design monitoring and verification.

U.S. Patent 6,161,189 issued to Arimilli et al teaches latch and hold snooper circuit.

U.S. Patent 6,378,123 issued to Dupenloup teaches ASIC design simulation and verification.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Fred Ferris whose telephone number is 703-305-9670 and whose normal working hours are 8:30am to 5:00pm Monday to Friday.

Any inquiry of a general nature relating to the status of this application should be directed to the group receptionist whose telephone number is 703-305-3900.

The Official Fax Numbers are:

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